

## **ABSTRACT OF THE DISCLOSURE**

A method and apparatus are described herein that may be used to provide the cost effective characterization of IO interconnections as simplified RC networks thus allowing for efficient testing of multiple different external interconnection topologies. In one embodiment the electrical characteristics of an IO interconnection are measured and characterized. A resistive-capacitive network is then designed so that it approximates the IO interconnection within some specified tolerance. The RC network may be fabricated on-chip between the driver and the receiver of an IO port or the RC network may be implemented on a PCB to facilitate production testing. In an alternative embodiment, closer approximation to the actual characteristics of the IO interconnection is achieved through the conjunction of several RC networks. Moreover, this process is repeatable for the emulation of multiple different links.